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Serial No. 09/648,164

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Chyan, Yih Feng
Hergenrother, John
Monroe, Donald

Case: 15-6-9

Serial No.: 09/648164

Filing Date: August 25, 2000

Examiner: Dickey

Group Art Unit: 2826

Title: Architecture for Circuit Connection Of A Vertical Transistor

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks Washington, D.C. 20231 on 1-10-02

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Mary V. Carter
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SIR:

Amendment Under 37 C.F.R. § 1.111

In response to the office action of April 10, 2002, please amend the above-identified application as follows:

IN THE SPECIFICATION

(1) Please replace the sentence at page 4, line 7 with the following: CMOS

line integrated circuits having PMOS transistors integrated with NMOS transistors are well known, and a process for fabricating CMOS vertical MOSFETs is described in U.S.

Serial No. 09/335646 entitled, "A CMOS Integrated Circuit Having Vertical Transistors and a Process of Fabricating Same," filed on June 18, 1999, now incorporated by reference.

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page 3, line 20
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